quilc The Rigetti Quil compiler

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Rigetti Quantum Computing

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Quil, the language

High-level

Assembly-like. Small set of instructions, qubit "registers".

DECLARE ro BIT[32] CNOT 0 1 RX(pi/2) 4 MEASURE 4 ro[4]

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RX(pi/2)	4	
MEASURE	4	ro[4]

Salient features

Portability Gate-based architecture assumed, not much else.

Hybrid prim. Language-level support for:

- yield-type functionality,
- simple classical reasoning,
- Image of the second second

Simplicity Simple grammar, simple semantics, minimal functionality.

quilc: A typical run

Main tasks

- Complex, high-level, device non-specific operations become simple, low-level, device-specific operations.
- Identify clever decompositions and deploy them. Identify unnecessary work and eliminate it.

quilc passes

Analyze CFG Segment "purely quantum" subprograms from intervening classical computation. Eliminate unnecessary logic.

Address Decompose complex operations and marry user-specified resources to target device resources.

Optimize Remove redundant gates.

Reconstitute Prepare program for transmission.

Each of these involves crawling the program in a distinct way.

Primary use case

Execution of advantage-class algorithms on our devices.

Supporting principles

- Monolithic operation
- Retargetability
- Production-grade software

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Monolithic operation

Problem: Interplay of passes in compiler makes it hard to predict the full effect of any particular optimization.

Redress: Encourage new interactions among new passes, and make the default mode of use cash in on these interactions.

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Case study: 2Q depth of random 4Q interaction on a line

gateset	old	QISKit challenge	all-to-all
CZ	230 (2.0x)	210 (1.82x)	115 (1.0x)
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Guess: CZ and ISWAP are "mirror gates": SWAP \equiv ISWAP \cdot CZ. **Try:** Weight ISWAP as twice CZ.

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 $\label{eq:Guess: CZ and ISWAP are "mirror gates": SWAP \equiv ISWAP \cdot CZ.$ Try: Weight ISWAP as twice CZ. Conclusion: Somehow, CZ + ISWAP + QISKit strategy actually does better than CZ + ISWAP or QISKit strategy on their own.

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Retargetability

Problem: Chips' intended design / actual features / operating points are in flux on timescales of months / weeks / hours.

Redress: Make it minimum-effort to target new devices.

Data

A "QPU graph" Σ : vertices are qubits, edges are qubit-qubit interactions. Each piece is tagged with native operations, their matrix encodings, execution properties (e.g., fidelity, duration),

$\mathsf{Data} \mapsto \mathsf{Strategies}$

Address Fixed set of strategies available, each suitable for dealing with any (perhaps irregularly) shaped device. Nativize/Optimize Starting from Σ 's native gate set, backsolve for compilation subroutines that rewrite an arbitrary program into the desired gateset.

Tiny example Σ with defa	nults
prog = """H	0
RY(pi/3)	0
RZ(pi/8)	0
RX(2*pi/5)	0"""
isa = {"1Q": {"0": None}}	

```
RZ(-2.06171187047457) 0 # Entering rewiring: #(0)
RX(pi/2) 0
RZ(1.656541137935280) 0
RX(-pi/2) 0
RZ(1.088693765816577) 0 # Exiting rewiring: #(0)
```

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$\boldsymbol{\Sigma}$ with free RXs, RZs

isa = {"1Q":	
{"0":	
[{"op": "RZ", "params": ["_"], "args": [0],
"fidelity": 0.99, "duration": 80},	
{"op": "RX", "params": ["_"], "args": [0],
"fidelity": 0.99, "duration": 80}]}}	

RX(-0.8789605131516703) 0 # Entering rewiring: #(0) RZ(-0.6433291804340883) 0 RX(-0.8994990281493116) 0 # Exiting rewiring: #(0)

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$\boldsymbol{\Sigma}$ with free RXs, RZs; preferring RZs

```
isa = {"1Q":
    {"0":
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        "fidelity": 0.999, "duration": 80},
        {"op": "RX", "params": ["_"], "args": [0],
        "fidelity": 0.99, "duration": 80}]}}
```

RZ(2.65067710991012) 0 # Entering rewiring: #(0) RX(1.65654113793528) 0 RZ(2.65949009261147) 0 # Exiting rewiring: #(0)

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Σ with free RXs, RZ($\mathbb{Z}\pi/2$)

```
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```

Condition CL-QUIL::NO-COMPILER-PATH was signalled.

Backtrace:

- 0: FIND-SHORTEST-COMPILER-PATH
- 1: COMPUTE-APPLICABLE-COMPILERS
- 2: WARM-HARDWARE-OBJECTS

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Teach quilc a new trick

```
(define-compiler RZ-to-XZXZX
  ((rz-gate (RZ (alpha) q)))
  (inst RX '( #.-pi/2) q)
  (inst RZ '( #.pi/2) q)
  (inst RX '(,(- alpha)) q)
  (inst RZ '( #.-pi/2) q)
  (inst RX '( #.pi/2) q))
```

```
RX(-2.449756839946568) 0 # Entering rewiring: #(0)
RZ(pi/2) 0
RX(0.6433291804340882) 0
RZ(-pi/2) 0
RX(0.6712972986455852) 0 # Exiting rewiring: #(0)
```

Question

For native gates Γ , howcan a gate G be written as $G = \gamma_1 \cdots \gamma_n$?

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A sort of answer (P.–Crooks–Smith)

For $\Gamma = \Gamma_{2Q} \cup \{1Q \text{ gates}\}$, *G* decomposes iff certain numerical invariants of *G* belong to a certain finite union of convex polytopes.



Some polytopes indicating when G decomposes, $1 \le k \le 5$:



Production-grade software

Problem: Compilers are *highly* complex pieces of software, prone to sprawl, slowness, tricky bugs,

Redress: Follow SWE best-practices: keep speed on the table, write highly extensible code, make using it feel like other compilers, build off of half a century of people thinking about compiler design.

Common Lisp pros

Exploratory Easy to feel out a poorly understood problem space.

Fast Very speedy executables.

Stable Extremely stable language definition. Compilers from the '80s are still a rich source of information today.

Extensible CL extends to cover the problem at hand, easing your colleagues' work (e.g.: define-compiler).

Common Lisp cons

Unfamiliar Physicists are reluctant to learn it. "My time is more valuably spent doing physics."

Insulated Interoperation with outside software requires attention: can be done, varies by implementation, isn't plug-and-play.

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quilc and Common Lisp

Common Lisp: Personal experience

- No opportunity to be skeptical at the start.
- Easy language to learn, except for the idioms.
- Right tool for the right job.[†]

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Michael Burge @TheMichaelBurge



f(5,6) - "The ideal syntax for practical programmers" f 5 6 - "Bizarre; only academics would use" (f 5 6) - "Too many parentheses" 5.f(6) - "Preferred for your next web app"

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Physicists

Likes Running benchmarks.

Dislikes Optimizing compilers / attempts to hide infidelity. Respecting abstraction boundaries. Using enough qubits to need an addresser.

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Applications engineers

Likes Hand-optimization. Maximum chip use.

Dislikes Software trampling their careful optimization.

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quilc in the wild

Newbies Likes Simply-described quantum programs. Wasting spatial resources. Dislikes Hardware limitations.

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Important observation

None of these are the supposed default of "advantage-class algorithms running on advantage-class Rigetti hardware".

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Interoperability: ECL and C-style bindings.

Pulse-level control: quilc to extend downward: everything but the back-most piece of the compiler backend.

Higher-level constructs: Hamiltonians instead of circuits, projection operators instead of σ_z -basis MEASUREs, automatic mechanisms to trade more resources for increased connectivity / stability /

"Exotic" gatesets: $XY(\theta)$, Google's goofy gate,

Thank you!!

http://github.com/rigetti/quilc http://rigetti.com http://chromotopy.org

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